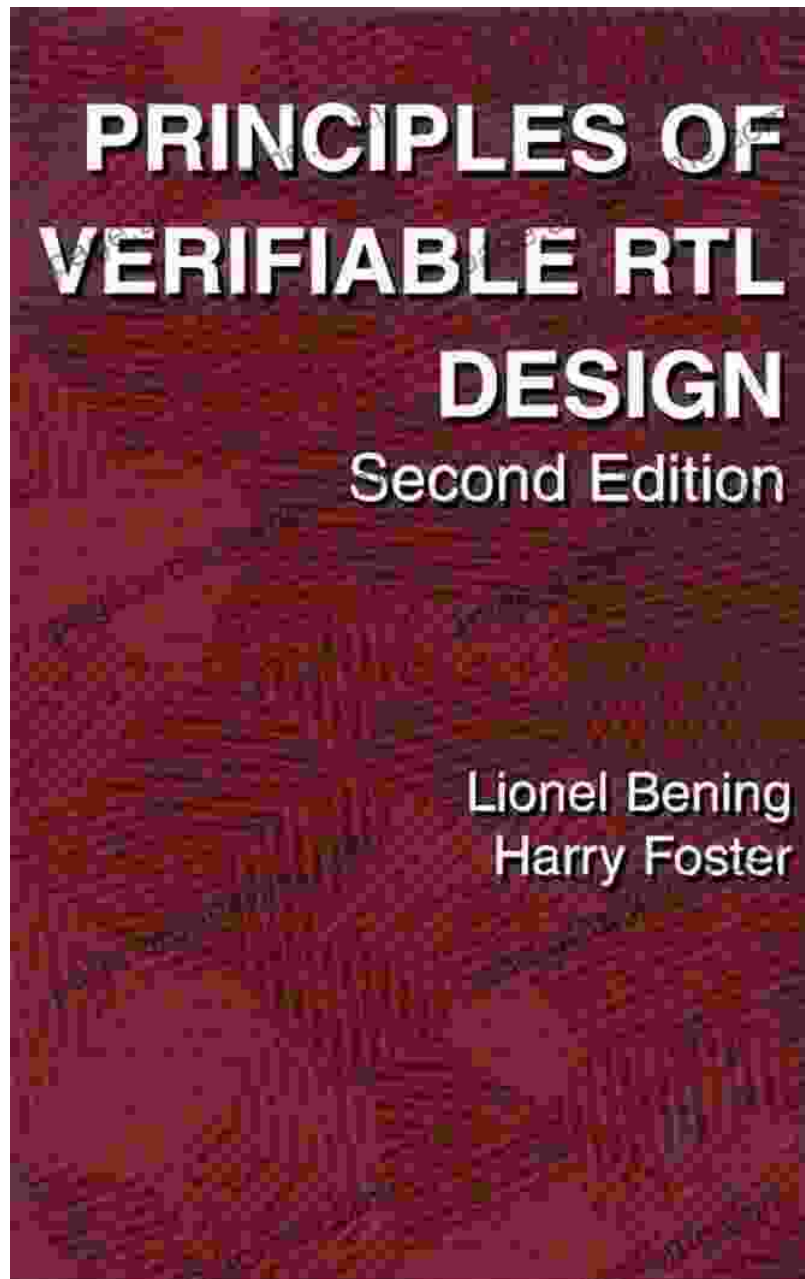
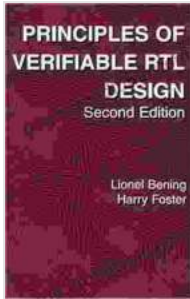


Principles of Verifiable RTL Design: A Comprehensive Guide to Achieving Verilog and SystemVerilog Functional Coverage



Principles of Verifiable RTL Design: A functional coding style supporting verification processes in Verilog



by Lionel Bening

★★★★☆ 4 out of 5

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Principles of Verifiable RTL Design is a comprehensive guide to achieving Verilog and SystemVerilog functional coverage. It covers all aspects of the RTL design process, from concept to implementation, and explains how to use formal methods to verify that the design meets its requirements.

The book is written by experienced ASIC and FPGA designers, and is full of practical tips and advice. It is essential reading for anyone involved in digital design.

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Reviews

"Principles of Verifiable RTL Design is a comprehensive guide to achieving Verilog and SystemVerilog functional coverage. It is a must-read for anyone involved in digital design."

- Prof. Michael Keating, University of Toronto

"Principles of Verifiable RTL Design is a valuable resource for anyone who wants to learn about formal verification. It is well-written and full of practical tips and advice."

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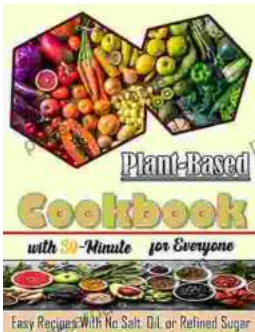
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